REMARKS

In response to the above-identified Office Action, Applicants amend the application and seeks reconsideration thereof. In this response, Applicants amend claims 1, 4, and 6. Applicants do not cancel any claims or add any new claims. Accordingly, claims 1-9 are pending.

I. Claims Rejected Under 35 U.S.C. § 112, second paragraph

Claims 1 and 4 stand rejected under 35 U.S.C. § 112, second paragraph. Claim 1 recites "a third means for maintaining a stabilized bias current by current mirror independent of changes of the control voltage." The Examiner asserts that any stabilization by the third means is in some small way dependent on the control voltage connecting to the gate of transistor P102, which constitutes part of the third means as recited in claim 4. Applicants thus delete the language "independent of changes of the control voltage" to promote clarity. Accordingly, reconsideration and withdrawal of the rejection of claim 1 and its dependent claim 4 are respectfully requested.

II. Claims Rejected Under 35 U.S.C. § 102

Claims 1, 2, 3, and 5 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,710,659 issued to Teramoto ("Teramoto"). Applicants respectfully traverse the rejection.

To anticipate a claim, the Examiner must show that a single reference teaches each of the elements of that claim. Amended claim 1 incorporates part of allowable claim 4 to recite:

> "...wherein the third means further comprises:
>
> a current source for supplying a given current,
>
> a first PMOS transistor driven by the bias voltage, for supplying the current from the current source, and
>
> a second PMOS transistor driven by the control voltage, for supplying the current from the current source."

Applicants submit that Teramoto does not teach these elements. Teramoto does not disclose any PMOS transistor driven by a bias voltage or a control voltage. Rather, the control voltage V_{AGC} taught by Teramoto connects to Q11, Q15, and Q16, all of which are NPN-type transistors.

Moreover, Teramoto does not explicitly teach any bias voltage applied to the disclosed circuit. Additionally, claim 1 incorporates patentable features of allowable claim 4. Thus, Teramoto does not teach each of the elements of claim 1.

In regard to claims 2, 3, and 5, these claims depend from independent claim 1 and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claim 1, Teramoto does not anticipate these claims. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 1, 2, 3, and 5 are requested.

III. Allowable Subject Matter

The Examiner has allowed Claims 7-9.

Applicants note with appreciation the Examiner's indication that Claims 4 and 6 would be allowable if rewritten in independent form. Applicants amend claim 6 to remove indefiniteness of the recited PMOS transistor, as necessitated by the amendment to claim 1. Claims 4 and 6 depend from Claim 1 and incorporate the limitations thereof. As Claim 1 is in condition for allowance for the reasons mentioned above, its dependent claims are allowable at least for the reasons mentioned in regard to Claim 1. Accordingly, reconsideration and withdrawal of the objection of Claims 4 and 6 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-9 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Erin Flynn October 25, 2005